Development Plan

Fri. 11/21

DONE -Determine Interface for modules: L1 Cache, L2 Cache, Main Memory

Module Naming Convention/ Variable Naming Convention

Capitalize words in module names

Use uppercase letters only for parameters with underscore

Use lowercase letters only for wire/net/variables with underscore

List Input first, Output next, Inout last in port list.

DONE-Finalize L1 and Main Memory Stub

Sat. 11/22

Comment each Code

Develop clear algorithm/flow chart:

Develop L2 Cache Module

Milestones

1. Generate Array ( Linesize = 2/ Index = 4/ Way = 1)
2. Address decoding (TAG, INDEX, Word Select)
3. Read a word from Cache
4. (Write a word to Cache)
5. Read cache line from DRAM